ABSTRACT

Aspects of saving power in a serial link transmitter are described. The aspects include providing a parallel arrangement of segments, each segment comprising prebuffer and output stage circuitry of the serial link transmitter and each segment enabled independently to achieve multiple power levels and multiple levels of pre-emphasis while maintaining a substantially constant propagation delay in a signal path of the serial link transmitter. Further aspects include providing a bypass path in the prebuffer stage circuitry to implement a controllable idle state in the segments and tail current and resistive load elements in the prebuffer circuitry as sectioned portions for slew rate control capability. Also included is provision of a control element with pre-emphasis delay circuitry in the transmitter signal path to allow inversion of a last delayed bit of the pre-emphasis delay circuitry to achieve a polarity change of a pre-emphasis weight.